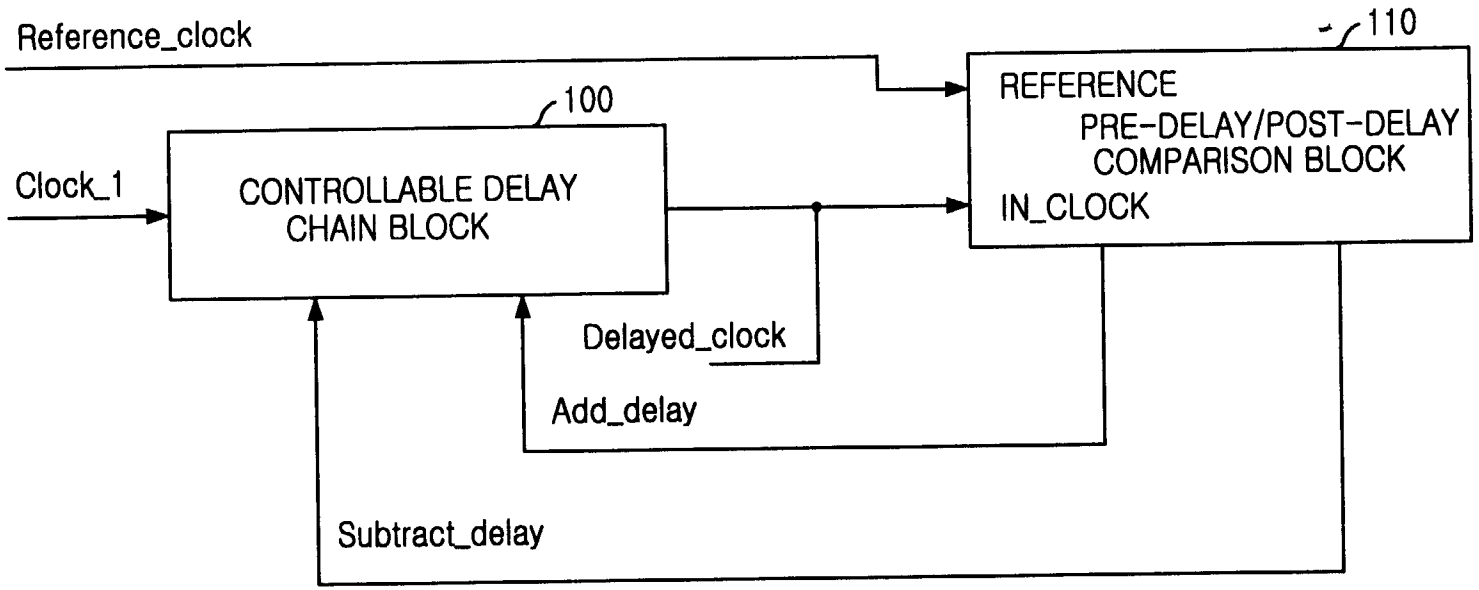
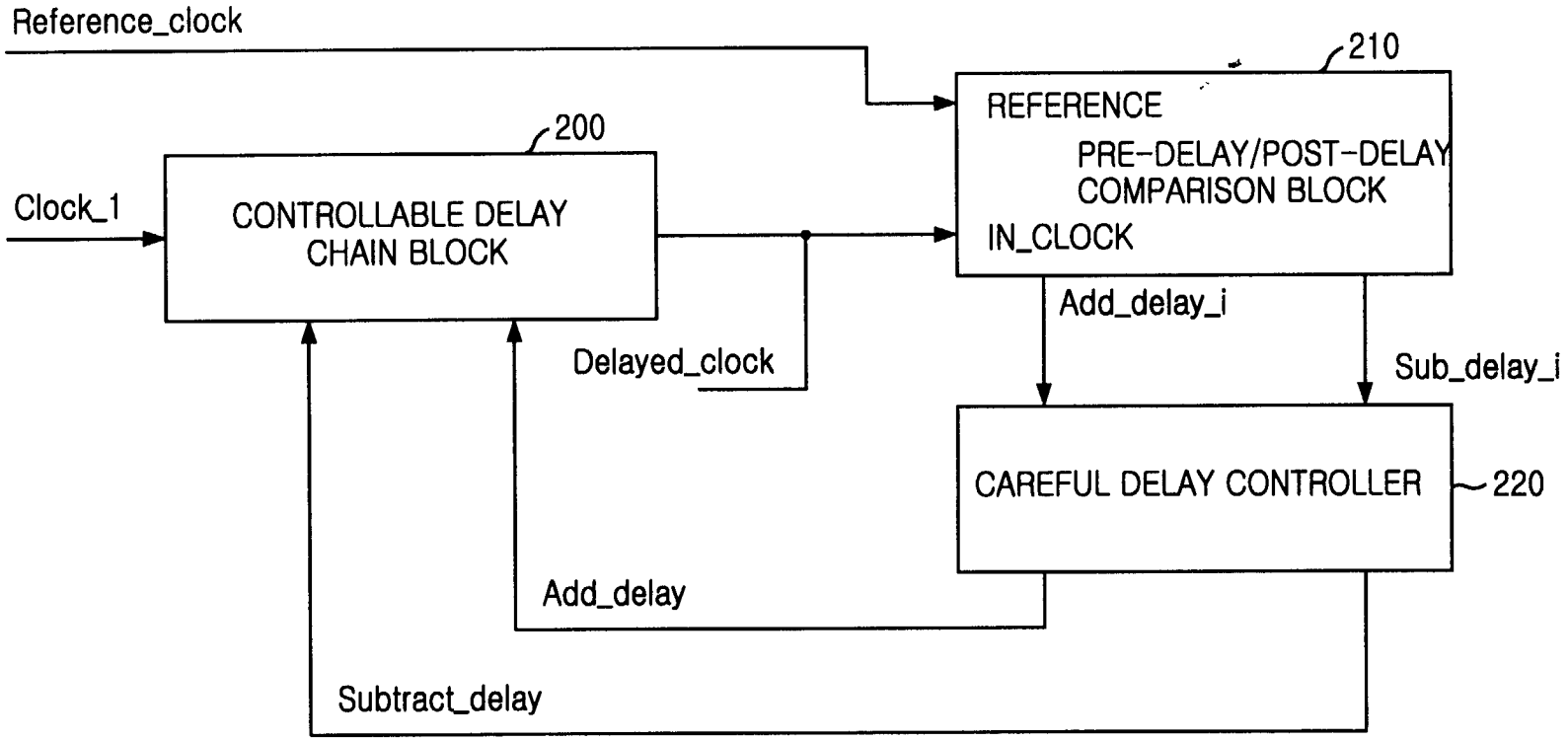
FIG. 1
(PRIOR ART)



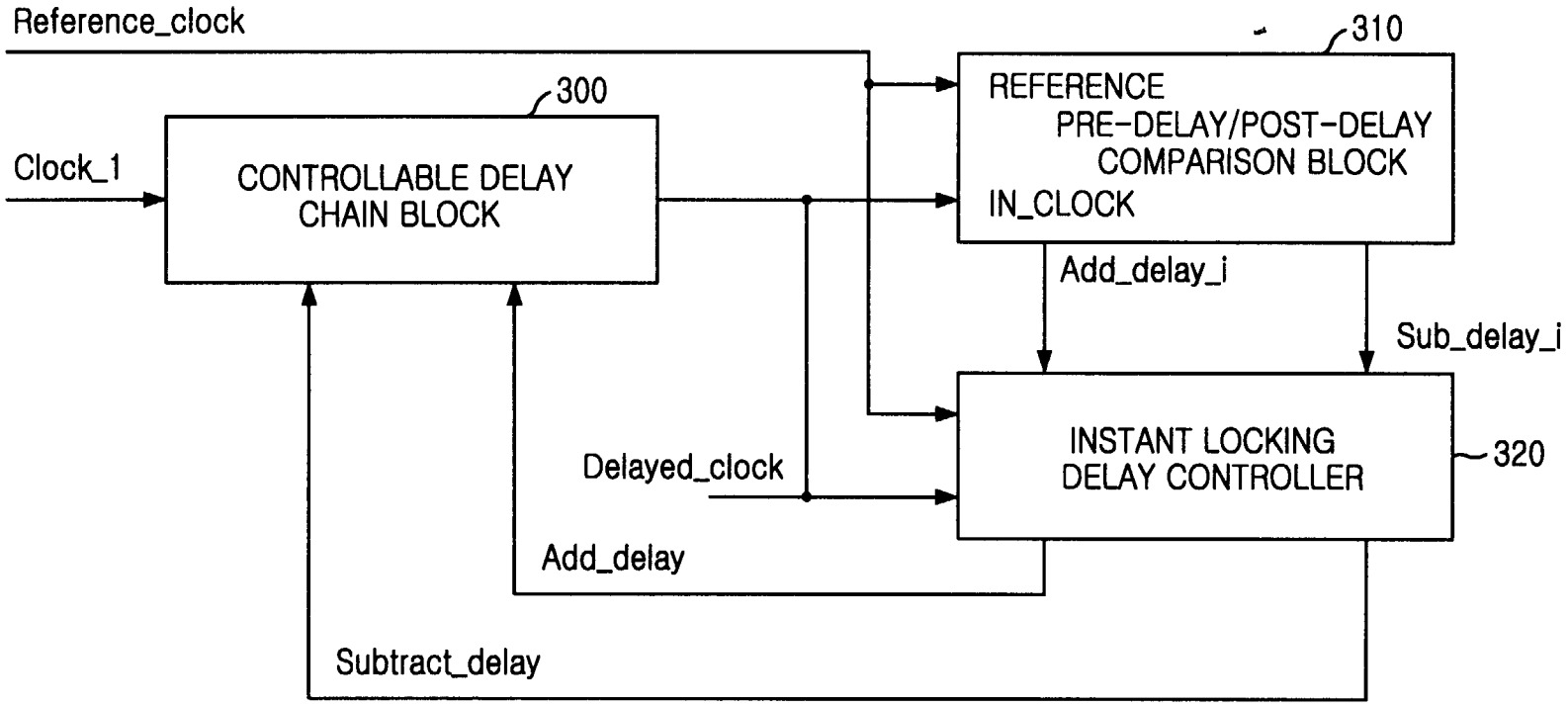
SCANNED # 4

FIG. 2
(PRIOR ART)



SCANNED, # 4

FIG. 3



SCANNED #

FIG. 4

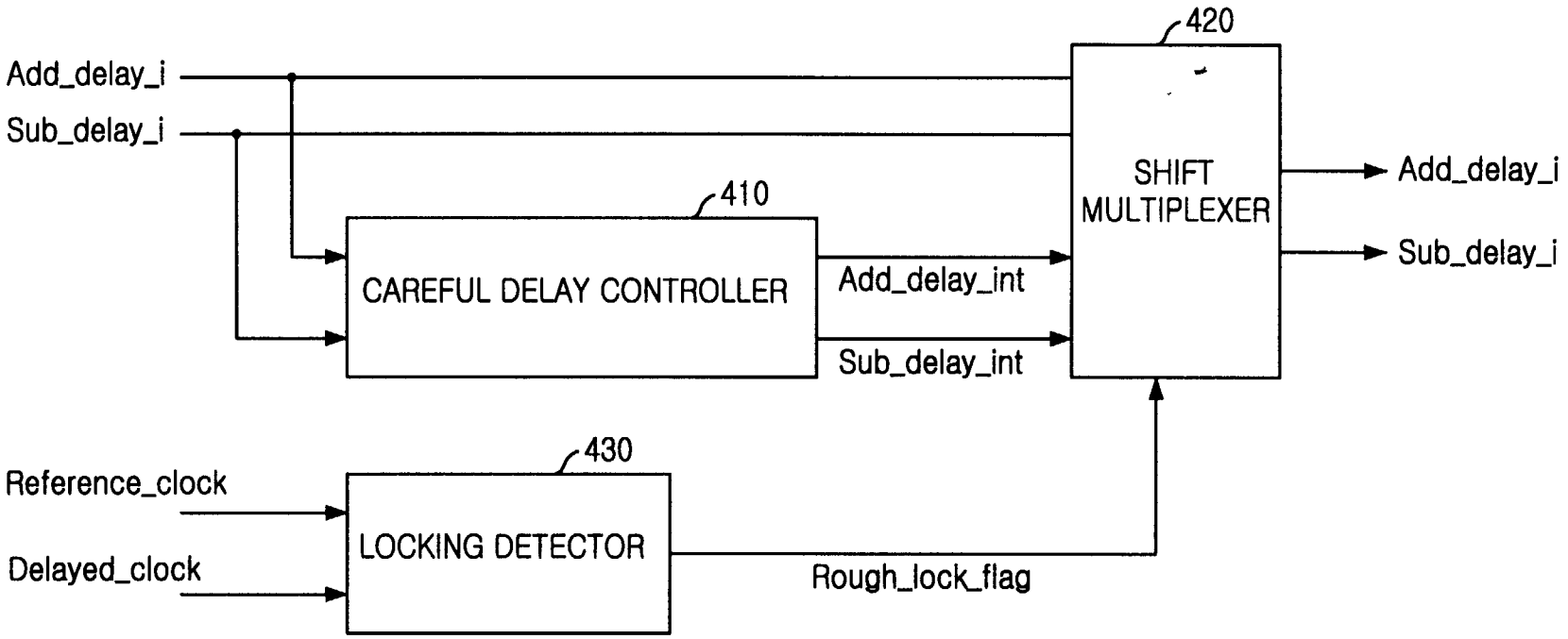
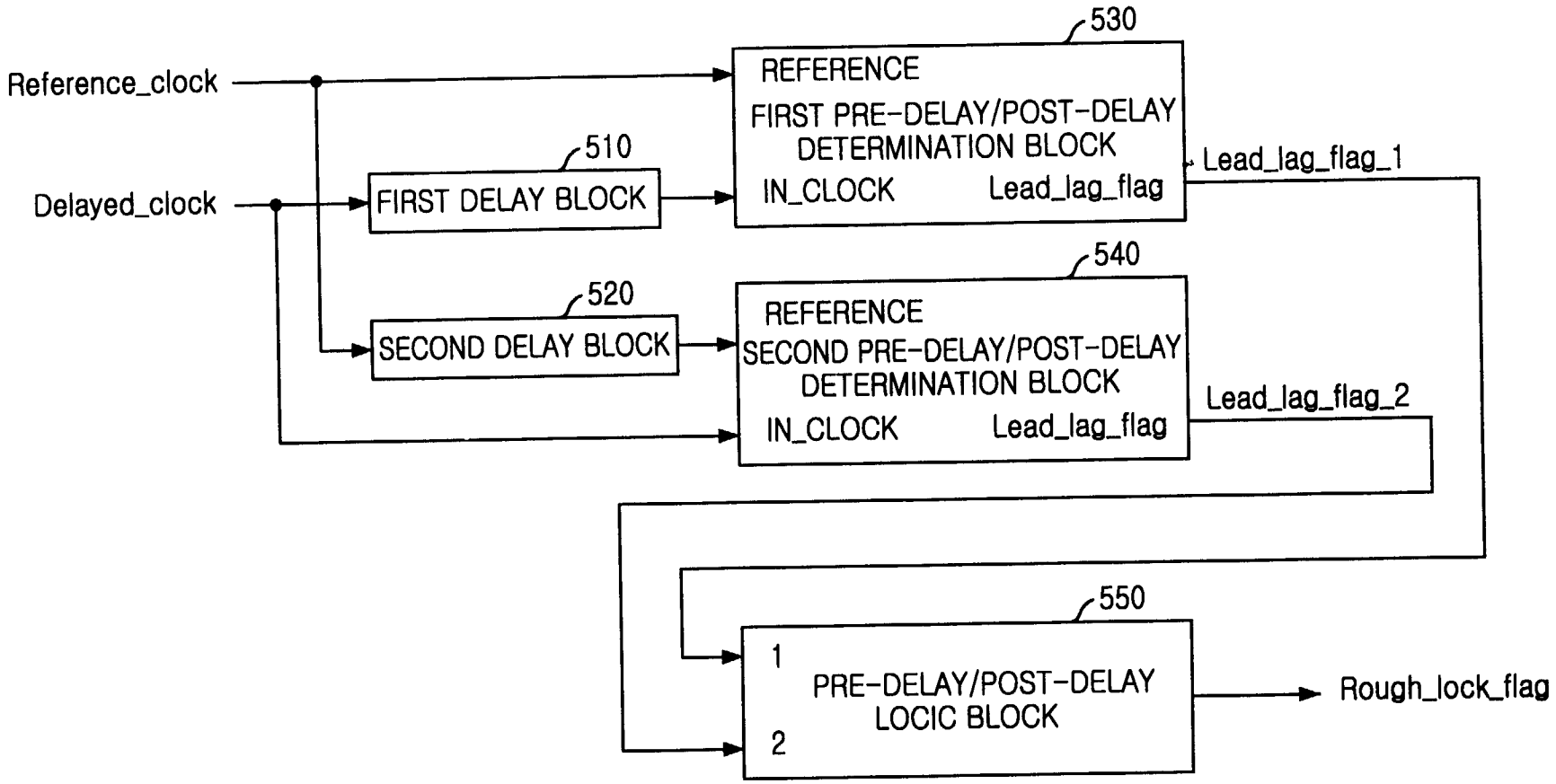


FIG. 5


Reference_clock
Delayed_clock
530
REFERENCE
FIRST PRE-DELAY/POST-DELAY
DETERMINATION BLOCK
IN_CLOCK
Lead_lag_flag
Lead_lag_flag_1
510
FIRST DELAY BLOCK
520
SECOND DELAY BLOCK
540
REFERENCE
SECOND PRE-DELAY/POST-DELAY
DETERMINATION BLOCK
IN_CLOCK
Lead_lag_flag
Lead_lag_flag_2
550
1
2
PRE-DELAY/POST-DELAY
LOCIC BLOCK
Rough_lock_flag

SCANNED, # 4

FIG. 6

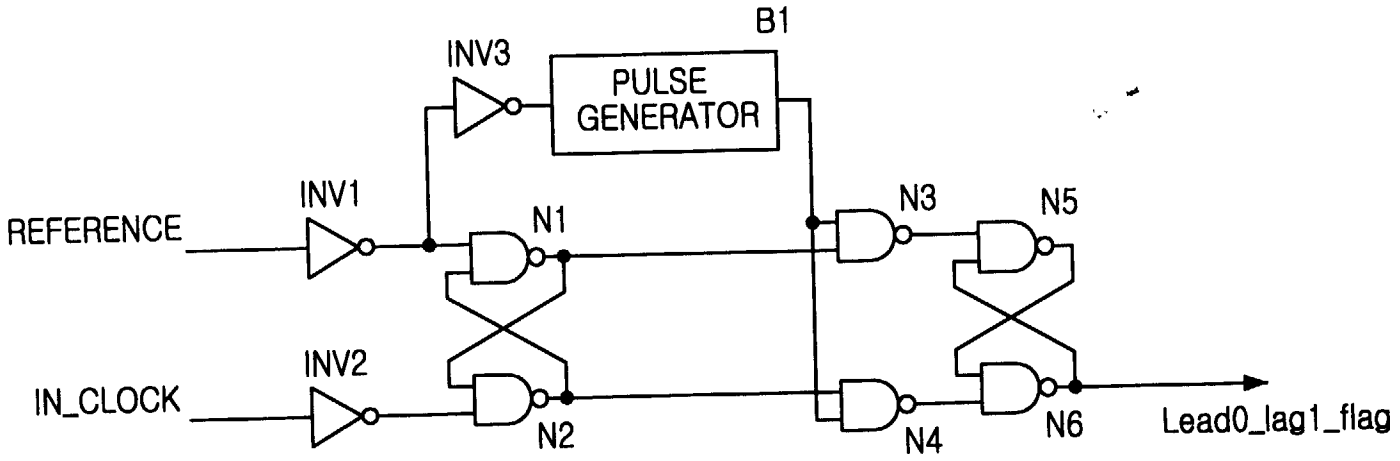
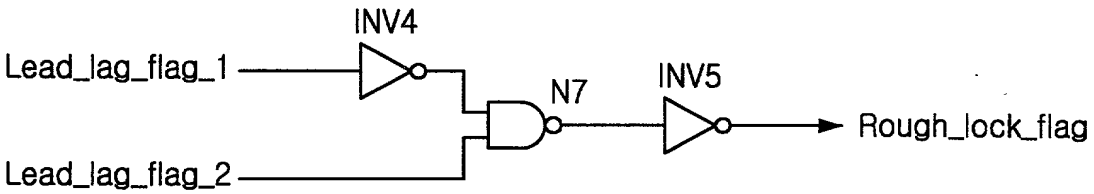
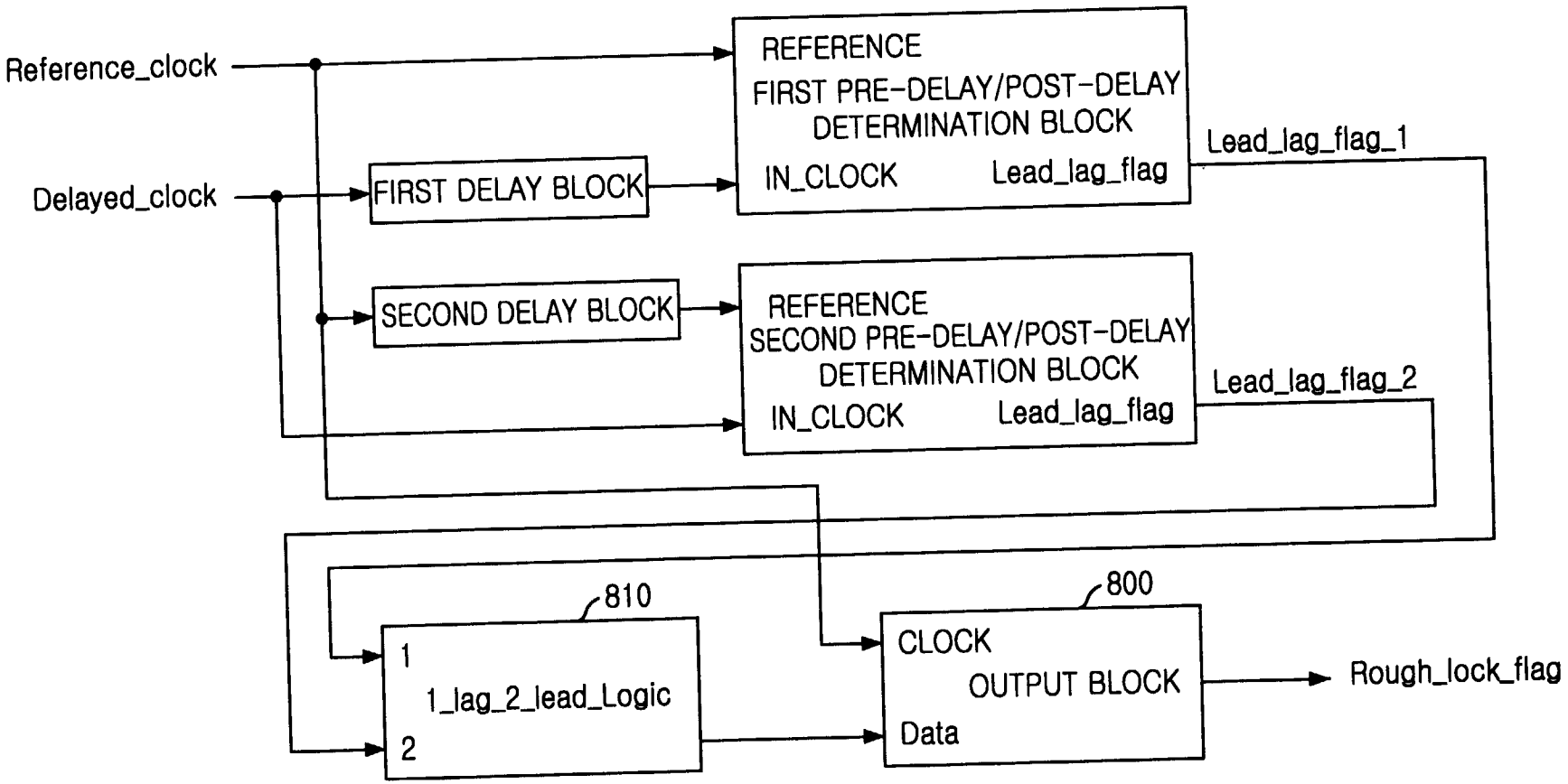


FIG. 7



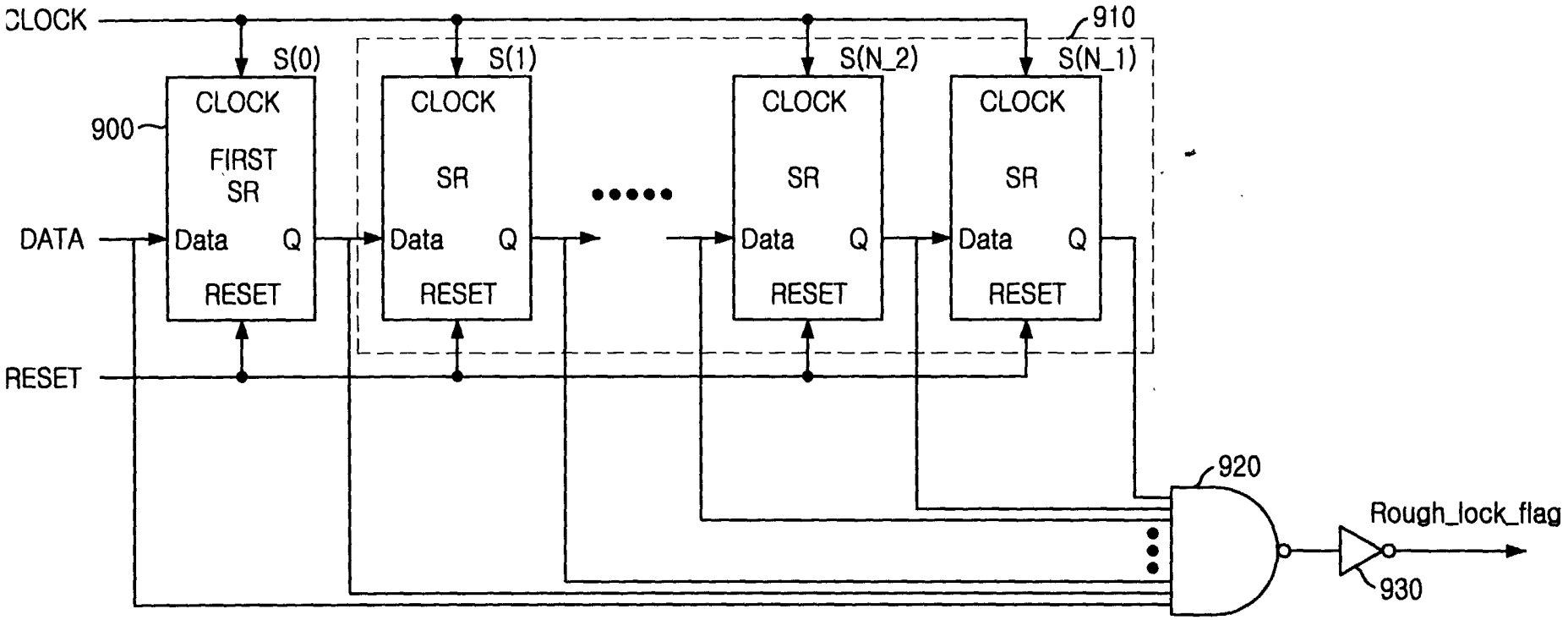
SCANNED, # 4

FIG. 8



SCANNED, # 4

FIG. 9



SCANNED, # 4

FIG. 10

